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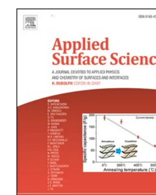

Full Length Article

Dislocation nucleation triggered by thermal stress during Ge/Si wafer bonding process at low annealing temperature

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ABSTRACT

We report nucleation of dislocations in Ge of Ge/Si bonded pairs annealed at low annealing temperatures (≤400 °C). Two types of dislocation networks are revealed near Ge/Si bonded interface for the first time, including sparsely distributed dislocations (type-I) and criss-crossingly arranged ones (type-II). A thin amorphous Si (a-Si) intermediate layer is introduced at the Ge/Si bonded interface to eradicate the influence of the lattice misfit between Si and Ge, and the thermal stress is proved to be the driving force for nucleation of both types of dislocation. Impact of annealing temperature on dislocation nucleation is identified. It is observed that type-I dislocations constitute the majority of dislocations in Ge wafer of bonded pairs annealed at annealing temperature range 275–350 °C, and type-II ones start to prevail at annealing temperature range 350–400 °C. A kinetic model that accommodates the strain relaxation process and behavior of dislocation is constructed based on fundamental strain and dislocation theory. By fitting the experimental data, it is proposed that heterogeneous nucleation caused by "initial nucleation sites" correlated with surface fluctuation and pretreatment is dominant for dislocation nucleation at low annealing temperature range, and multiplication mechanism activated by secondary nucleation sites, such as Frank-Read sources, incurs the booming of dislocation density (DD) at elevated temperatures. This finding may cast light on the nature of crystallinity degradation of Ge wafers integrated on Si substrate by a hybrid wafer bonding technology.

1. Introduction

Si based electro-photonic integrated circuits (Si-OEIC), featuring high data rates, low thermal dissipation, and immunity to parasitic effect, have been considered as one of the most promising candidates for next generation high-density integration techniques where data exchange rate exceeds 10 Gb/s. Germanium, possessing high carrier mobility, high absorption in near infrared communication band, and compatibility to the matured standard Si fabrication technology, has been aggressively researched for its potential application in photoelectric devices. Extensive efforts has been devoted to obtain effective Ge/Si heterogeneous integration which will enable efficient photo-electric conversion process in Si-OEIC network system [1,2]. However, due to 4.2% lattice misfit between Si and Ge, high quality hetero-epitaxy of Ge on Si-based substrate still remains difficult task. DD as high as 10^6 cm^{-2} is demonstrated in Ge epitaxial layers obtained by traditional growth methods such as molecular beam epitaxy (MBE), chemical vapour deposition (CVD), and liquid phase epitaxy (LPE) [3].

Recently, wafer-bonding techniques such as hydrophobic bonding [4], hydrophilic bonding [5,6], and plasma-aided bonding [7,8] emerge as novel hybrid integration techniques which are designed to circumvent bottlenecks of epitaxy scheme by directly bonding two perfect crystalline wafers together. Assisted by Smart Cut^{TM} technology, Ge films have been transferred to Si-based substrate successfully with little voids and high bonding strength [9-11]. No dislocation is yet found, mostly during Transmission Electron Microscopy (TEM) examination, in Ge/Si hetero-structure materials fabricated by low temperature bonding (<400 °C). This leads the majority to believe that defect-free Ge film on Si-based substrate is successfully fabricated by bonding techniques [5,12-14]. However, paradoxically, photo-electronic devices based on bonded Ge/Si heterostructures generally own much higher leakage current density than those fabricated by bulk Ge. Further analysis shows

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that leakage current of bonded Ge/Si photodiodes is mainly generated by trap-assisted generation recombination process. This suggests that a certain number of dislocations may be nucleated in transferred Ge while they were neglected by previous researches [11,15-17].

Several research groups have revealed dislocations in Ge/Si bonded pairs and speculate that thermal stress [18,19], lattice misfit [5,6], and grown-in dislocations [20] may be the driving force for dislocation nucleation. However, annealing process at temperature higher than 600 °C is mostly implemented in their research. Moreover, none of these groups has revealed any notable correlation of dislocations in Ge with these suspected initiators listed above, and no affirmative conclusion has been reached. Up till now, mechanism concerning how the quality of Ge degrades during the bonding process still remains neglected and unclear.

In this paper, crystallinity degradation of Ge wafer of Ge/Si bonded pairs annealed at low annealing temperature is reported. Two kinds of dislocation networks are revealed. To eradicate the influence of stress induced by lattice misfit, the Ge and Si wafers are bonded with the aid of a sputtered a-Si intermediate layer. The influence of thermal stress on strain relaxation and behavior of dislocations in Ge/Si bonded pairs annealed at low annealing temperatures (<400 °C) is identified. A theoretical kinetic model related to strain relaxation process and dislocation nucleation in Ge/Si bonded pairs is proposed.

2. Experimental details

(001)-oriented Si substrates (2 × 2 cm, ~5 Ω cm, 500 μm) were chosen as handle wafer and cleaned with standard RCA and HF treatment. Double-side polished Ge (2 × 2 cm, 380 μm) wafers were chosen as donor wafer and cleaned with diluted HCl and HF treatment. After Si and Ge wafers were loaded into vacuum chamber, a thin a-Si film was deposited by magnetron sputtering at a background pressure of 7 × 10^{-5} Pa at room temperature. Then, the Ge and Si wafers were immersed into the diluted aqueous ammonia (1 mL NH_4OH : 10 mL H_2O) for 30 s before they were pre-bonded. Finally, the Ge/Si bonded pairs were annealed in the furnace to enhance bonding strength.

Ge/Si bonded interface was identified by TEM. Voids were examined by the C-mode scanning acoustic microscope (CSAM) with a frequency of 250 MHz. The AGS-X 5KN electronic universal testing machine was used to measure the bonding strength. Surface morphology of Ge surface was examined by atomic force microscope (AFM). Etch pits of dislocation were developed by Iodine etching solution (100 mL CH_3COOH : 40 mL HNO_3 : 10 mL HF : 30 mg I_2), and DD was checked by optical microscope and AFM.

3. Results and discussion

Fig. 1 illustrates the schematic diagram of the fabrication process of Ge/Si bonded pairs. The a-Si film was sputtered at room temperature to avoid any damages caused by thermal shock on Ge and Si wafers. Hydrophilicity of a-Si surface can be largely enhanced after the dip in diluted aqueous ammonia [21]. Cooling and heating rate during the annealing process was fixed at 0.5 °C min^{-1} to avoid possible temperature inhomogeneity of bonded pairs.

As shown in Fig. 2(a), the root mean square (RMS) roughness of a-Si surface is 0.21 nm, indicating that the surface of the sputtered a-Si film is flat enough to facilitate the bonding procedure. Ge/Si bonded pairs with intermediate a-Si layer of different thickness were fabricated. As shown in Fig. 2(b)-(e), distribution of bubbles at the interface of samples annealed at 400 °C for 5 h was examined by CSAM. One can see that when the thickness of sputtered a-Si film is <5 nm, bubbles incurred by gaseous byproduct are formed and trapped at the interface. Fortunately, as the thickness of a-Si increases, bubble density gradually decreases. And the bubbles can be totally eliminated when the sputtered a-Si thickness reaches 5 nm. This may be ascribed to the fact that the sputtered a-Si is loose and porous, and the gaseous byproduct can be absorbed by a-Si intermediate layer. Fig. 2(f) shows the high-resolution TEM (HR-TEM) image of the bonded interface of the sample with 5 nm sputtered a-Si after being annealed at 400 °C for 20 h. One can see that the a-Si intermediate layer is uniformly sandwiched between Ge and Si. The sharp lattice fringes of {1 1 1} planes of both Ge and Si wafers are clearly observed, demonstrating the perfect alignment of lattice orientation of two wafers during bonding process. The inset in Fig. 2(f) shows the Fast Fourier Transform (FFT) analysis of the HR-TEM image. It can be readily verified that the intermediate Si layer shows stable amorphous phase at temperature as high as 400 °C, indicating that lattice of

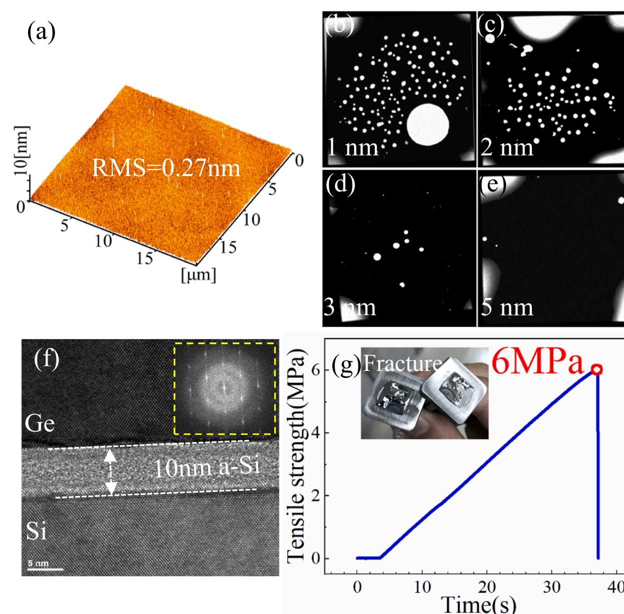

Fig. 2. (a) AFM image of sputtered a-Si film. (b)-(e) shows the CSAM images of bubble distribution at interface of Ge/Si bonded pairs with sputtered a-Si film of different thickness. The black part denotes the bonded areas and white part the voids. (f) HR-TEM image of Ge/Si bonded interface. Inset shows the FFT analysis of HR-TEM image. (g) Bonding strength of Ge/Si bonded pairs. Inset shows the fracture surface after the pull test.

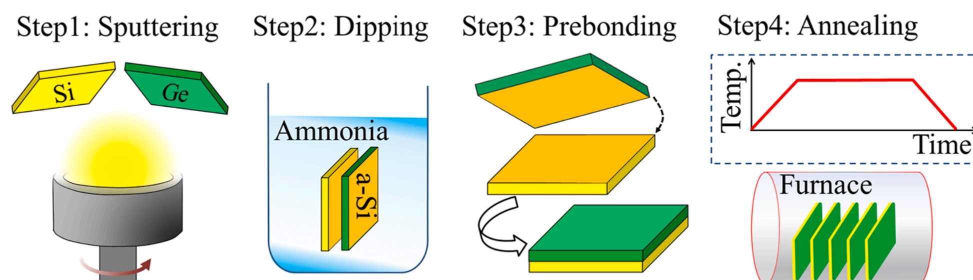

Fig. 1. Schematic diagram of Ge/Si wafer bonding process assisted by a-Si intermediate layer.

Ge and Si could be successfully separated during annealing duration. Tensile strength applied on the bonded pairs as a function of time during the pull test was shown in Fig. 2(g). It can be observed that bonding strength as high as 6 MPa is identified. The inset shows the fracture surface after pull test. It can be seen that the Ge/Si bonded pair split at Ge side, indicating a bonding strength higher than the fracture strength of bulk Ge.

The Ge/Si bonded pairs annealed at 325℃ for 5 h were immersed in Iodine etchant to develop etch pits on Ge surface. Calibrated etch rate of Ge in Iodine etchant is 20 nm/s. By varying the etch time, DD at different depth from the Ge surface can be obtained. Fig. 3(a)-(f) illustrate the evolution process of etch pit morphology. One can see that the etch pits are revealed when etch time exceed 100 min. Moreover, two types of dislocation networks are demonstrated as etch time increases. Only randomly-distributed type-I dislocations with round etch pits can be observed when etch time is less than 180 min. Criss-crossingly arranged type-II dislocations with fin-shaped etch pit, emerge when etch time is more than 240 min. Besides, type-II dislocations are lined transversally and longitudinally along the ⟨1 1 0⟩ direction on (0 0 1) Ge surface. It can be seen that when the etch-front approaches the Ge/Si bonded interface, type-II dislocation become more and more popular. Fig. 3(f) shows the morphology of Ge surface after being etched for 300 min. One can see that partial Ge is completely removed, and the Si wafer is exposed to the air. Note that part of etch pits are also transferred onto Si surface by the masking effect induced by Ge. Magnified view of two different etch pits is presented in Fig. 3(g). Two types of etch pits can be readily discerned. The asymmetrical shape of etch pits indicates that dislocation line of type-I I is inclined to Ge (0 0 1) surface, while type-I dislocations with round pits should own nearly vertical dislocation line. The DD as a function of the etch depth is plotted in Fig. 3(h). It can be seen that etch pits start to form at a distance of 300 μm from Ge/Si interface, indicating that the dislocation line expands from the bonded interface to nearly whole Ge wafer. The DD increases first and then stabilize as the etch-front approaches the Ge/Si interface.

The dislocation network presented above implies that the quality of Ge wafer deteriorates when bonded to Si. Due to the fact that the Ge and Si lattices are separated by a-Si, it is reasonable to deduce that the thermal stress caused by the difference of coefficient of thermal expansion (CTE) between Si and Ge materials is the driving force that triggers nucleation and expansion of dislocations in Ge wafer. In order to further investigate the influence of thermal stress on the behavior of dislocations, etch pits on Ge surface of Ge/Si bonded pairs annealed at different temperatures for 5 h were studied. Moreover, Ge/Ge bonded pairs with the Si handle wafer substituted by Ge wafer (450 μm) were fabricated in the same process flow for comparison. The compliant Ge handle wafer would abate the thermal stress in the bonded pairs. In addition, before annealing, all the Ge donor wafers are thinned to ~ 25 μm after the pairs were pre-bonded to prevent them from cracking and splitting at elevated annealing temperatures.

Fig. 4(a)-(d) illustrate the AFM images of Ge surface of Ge/Si bonded pairs which are annealed in temperature range 325–400 °C. As shown in Fig. 4(a), surface of Ge remains flat when annealing temperature is lower than 350 °C. Fig. 4(b)-(d) show that surface flatness of Ge gradually deteriorates as the annealing temperature increases. It can be seen that crosshatch patterns aligned along ⟨1 1 0⟩ direction start to prevail on Ge surface, indicating consistent slipping process of {1 1 1} planes in Ge [22-24]. As the Ge and Si wafers are separated by the a-Si intermediate layer, internal stress induced by the lattice misfit is eradicated. Hence, we propose that the thermal stress is the key force driving the slipping of {1 1 1} planes in Ge. This can be further supported by the fact that none crosshatch pattern was found on Ge donor wafer surface of Ge/Ge bonded pairs at whole annealing temperature regime.

Fig. 5 shows the etch pits on Ge of Ge/Si bonded pairs annealed at temperature range of 275–400 °C. The insets in Fig. 5(e)-(f) are AFM images of the local etch pits of samples annealed at 375 °C, and 400 °C. As shown in Fig. 5(a)-(d), type-I dislocations constitute the majority of

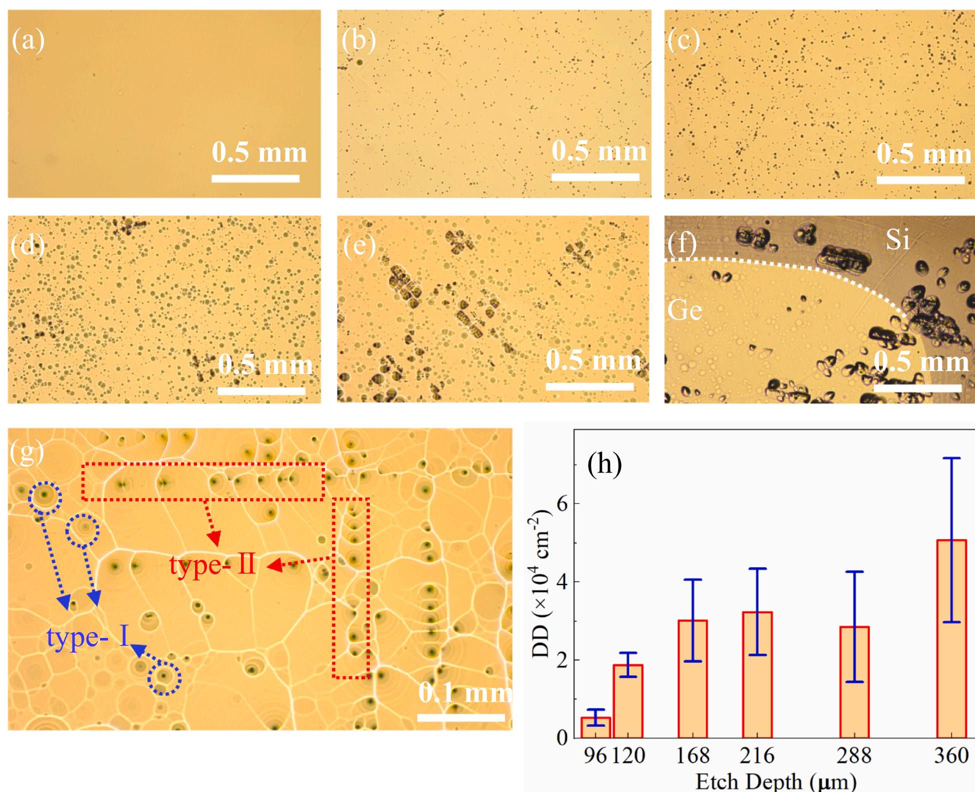

Fig. 3. Etch pits on Ge of samples that are etched for (a) 60 min, (b) 100 min, (c) 140 min, (d) 180 min, (e) 240 min, and (f) 300 min. (g) Magnified image of two kinds of etch pit networks. (h) DD versus etch depth.

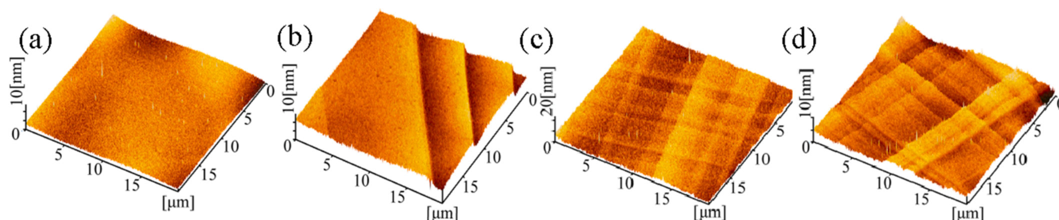

Fig. 4. Surface morphology of Ge of Ge/Si bonded pairs annealed at (a) 325 °C, (b) 350 °C, (c) 375 °C, and (d) 400 °C.

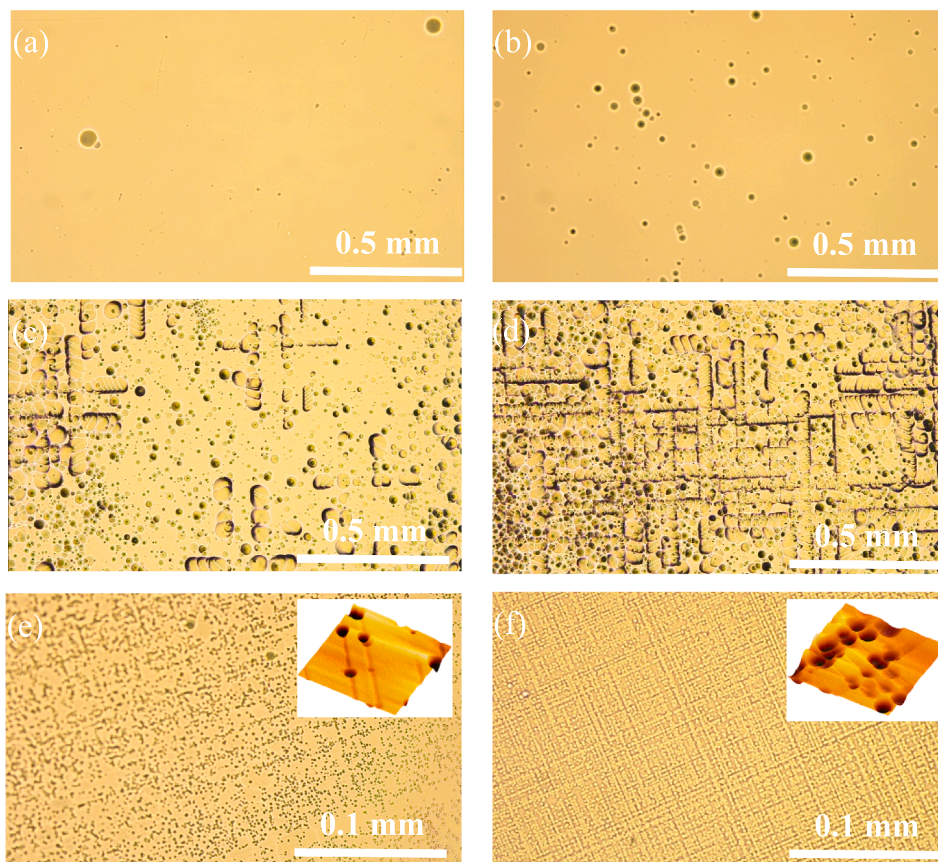

Fig. 5. Etch pits on Ge of Ge/Si bonded pairs annealed at (a) 275 °C, (b) 300 °C, (c) 325 °C, (d) 350 °C, (e) 375 °C and (f) 400 °C. Insets in (e)-(f) represent the AFM image of etch pits over a scope of 10 × 10 μm.

dislocations at relatively low annealing temperature range 275–350 ℃. Type-II ones start to form at 325 °C and become more and more popular as annealing temperature increases. When annealing temperature is higher than 350 ℃, type-II dislocations are observed in the whole detected scope. Statistically, total DD increases from 3×10^3 cm^{-2} to 2×10^7 cm^{-2} when the annealing temperature increases from 275 ℃ to 400 ℃. By contrast, no etch pits is observed on Ge surface of Ge/Ge bonded pairs in the whole annealing temperature range, indicating that it is the thermal stress that evokes the nucleation of dislocation.

Strain distribution in Ge/Si bonded pairs annealed at different temperatures was calculated by finite element method (FEM). Key calculation parameters are tabulated in Table 1. Fig. 6 shows in-plane component of elastic strain in the proximity of Ge/Si bonded interface during constant temperature period of the annealing process. One can see that magnitude of elastic strain in both the Ge and Si reaches the maximum at the bonded interface. The Si wafers are subjected to very slight tensile strain, while Ge wafers are compressively strained to a certain extent. Absolute value of strain in Ge surpass that in Si by one order of magnitude, indicating that the thermal stress exerts little influence on the Si wafer, while the Ge wafer is deformed more seriously. As shown in the inset of Fig. 6, the average compressive strain in Ge is positively correlated with annealing temperature and peaks at ~ 0.11%

Table 1
Key parameters used to resolve the elastic strain distribution in Ge/Si bonded pairs.

	CTE (C^{-1})	Young's modulus (GPa)	Poison's Ratio
Ge	$\alpha_{Ge} = 6.05 \times 10^{-6} + 3.6 \times 10^{-9} - 0.35 \times 10^{-12} T^2$ [26]	130	0.27
Si	$\alpha_{Si} = (\{1 - exp[-5.88 \times 10^{-3}(T + 149.15)]\}) \times 3.725 + 5.548 \times 10^{-4} T) \times 10^{-6}$ [26]	103	0.28
a-Si	3×10^{-6} [27]	87 [28]	0.31 [28]

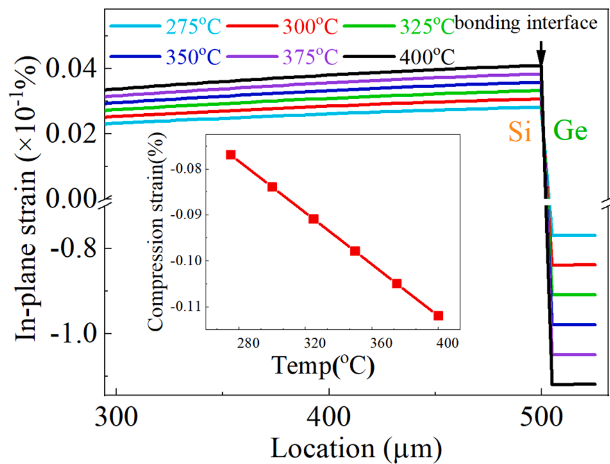

Fig. 6. Distribution of in-plane strain near Ge/Si bonded interface. Inset shows average compressive strain in Ge versus annealing temperature.

when the bonded pair is annealed at 400 °C.

Nucleation of dislocations in Ge/Si bonded pairs under relatively low annealing temperatures (≤400 °C) has not been researched before, and it is out of expectation that extensive dislocations as dense as 2×10^7 cm^{-2} are nucleated in Ge. It is opposite to the commonly accepted opinion that a stress comparable to around 1/30 of Ge's shear modulus is needed to trigger the nucleation of dislocation [25].

Massive researches concerning mechanism of strain relaxation and dislocation nucleation in diamond semiconductor have been conducted, and various models have been proposed such as mechanical equilibrium model by Matthews [29], direct nucleation model by People and Bean [30], and half loop nucleation model by Maree [31]. However, those models mainly concentrate on the stress induced by lattice misfit, and it is deemed that thermal stress is so trifling compared to the 4.2% misfit in lattice that it can be neglected when$\Delta T < 1000$ ℃. Furthermore, it is stressed that for Ge film under low strain ($<2 \times 10^{-3}$) nucleation of dislocation is suppressed by mobility effects. That is quite different from the phenomenon reported in this work. Dodson-Tsao further demonstrated that strain relaxation in strained Ge film on Si was determined by excess stress instead of the lattice mismatch [32,33]. Dodson-Tsao's theory correlates strain relaxation and behavior of dislocation with strain status of Ge film for the first time. However, their model predicts that a far more large strain value (above 0.5%) than the scope explored in this work is needed to trigger the relief of excess stress in bonded Ge/Si pairs. Moreover, interaction of dislocation and influence of the thermal stress are both ignored in their model.

To clarify the mechanism of dislocation nucleation in Ge, analysis based on the fundamental theories relating to dislocation behavior and strain relaxation in diamond semiconductor is conducted as follows. As the actual dislocation structures might be extremely complex and interactions between them sophisticated, our model mainly concentrated on the most common and widely debated 60° 1/2 ⟨1 0 1⟩ mixed type in diamond semiconductor for simplicity.

Firstly, based on energy equilibrium theory, by calculating the variation of system free energy caused by dislocation nucleation and strain relief, DD in Ge under an equilibrium state can be estimated on condition that reduction of free energy reaches its maximum [34]:

$$\frac{\partial U_{total}}{\partial N} = \frac{\partial (U_{strain} + U_{dis})}{\partial N} = 0 \quad (1)$$

where N is value of DD, U_{total} is total energy, U_{strain} is the strain energy, and U_{dis} is energy of dislocation network. As shown in Fig. 7(a), this model predicts an equilibrium DD exceeding 10^9 cm^{-2} which is larger than our experimental data by 2–4 orders of magnitude. This indicates that a kinetic mechanism, in which the nucleation of dislocation is hindered by an activation barrier, may be dominant for the strain relaxation process in Ge/Si bonded pairs. Considering the case of homogenous nucleation, variation of free energy of a single dislocation can be expressed as

$$\Delta E = E_{\sigma} - E_{dis} \quad (2)$$

where E_{dis} is energy of a dislocation loop, and E_{σ} is strain energy relaxed by the dislocation loop. [35,36] The activation barrier equals maximum of ΔE during the expanding process of dislocation loop. Fig. 7 (b) shows ΔE versus the radius of dislocation loop. One can see that extremely high activation energies up to thousands of eV are extracted for dislocation nucleation in Ge wafer of samples annealed at temperatures lower than 400 °C, implying that the homogeneous nucleation process of dislocation loops in Ge/Si bonded pairs is impossible.

Based on the analysis above, we propose that heterogeneous nucleation may be the principal mechanism of dislocation nucleation in the Ge/Si bonded pairs. It is considered that traps and damages caused by the a-Si sputtering, surface modification, and annealing may act as the initial nucleation site of dislocations. These nucleation sites will greatly lower the activation energy for dislocation nucleation which can be triggered by the thermal stress during the annealing process. Two kinds of nucleation models are presented here to clarify the structures of dislocations obtained at different annealing temperature regimes. At low temperature regime, Ge is lightly compressed as shown in Fig. 8(a) and Fig. 8(c). With the formation of Si-O-Si covalent bond, Ge and Si surfaces are towed closely, and local height fluctuations on both sides are deformed to fit each other tightly. Imperfections in surface flatness will make the thermal stress distribute unevenly in Ge [37]. On the other hand, it has been suggested that pretreatment will result in an inhomogeneous bonded interface [38,39], and it is highly possible that sudden change in thermal stress will occur at borders of areas with different bonding status. We speculate that local maximums in thermal stress caused by both those two reasons spur the dislocation nucleation

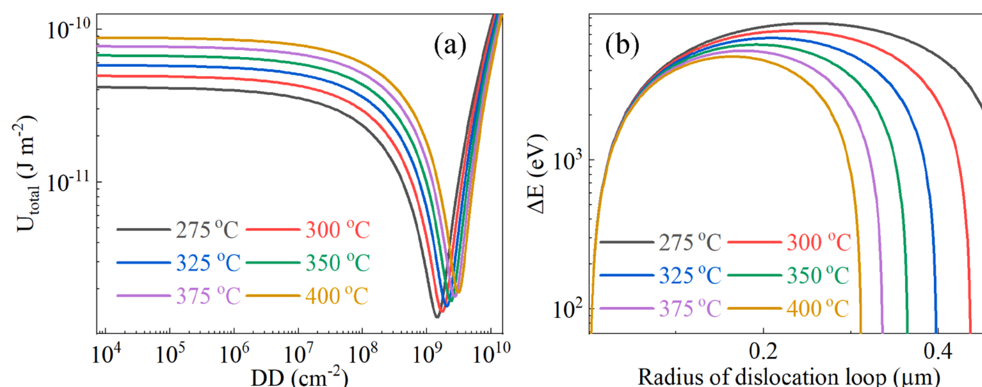

Fig. 7. (a) Energy density of Ge versus DD. (b) Variation of free energy versus radius of dislocation loop during homogeneous nucleation process.

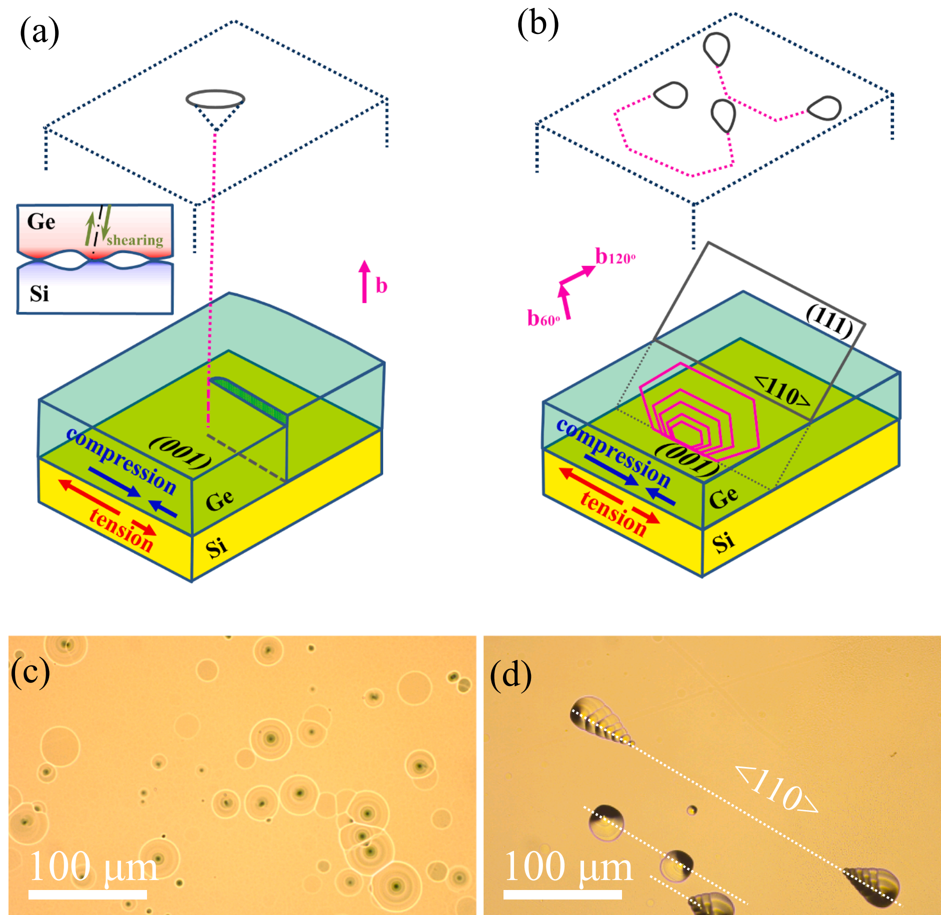

Fig. 8. Formation mechanism of (a) type- I and (b) type- II dislocations. Dashed lines show how etch pits are formed. Etch pits of (c) type- I and (d) type- II dislocations obtained in experiment.

at the vicinity of nucleation sites in Ge. As the surface fluctuations and areas with different bonding status are often randomly distributed, dislocations formed in this case are rambling as shown in Fig. 5(a)-(c). As shown in Fig. 8(b) and Fig. 8(d), at elevated annealing temperatures, Ge wafer is seriously compressed, and the propagation of dislocation becomes faster and easier. Secondary nucleation sites, such as Frank-Read sources, are created by the interaction of moving dislocations, facilitating the multiplication and pile-up of dislocation segment on {1 1 1} slip planes [40]. Extensive gliding and shuffling process of dislocations along the slip planes enable the dislocation loops to expand to Ge surface, giving rise to surface steps and crosshatch patterns as shown in Fig. 4. Etch pits formed in this case is criss-crossingly sequenced because the intersection lines of {1 1 1} slip planes and (0 0 1) Ge surface are longitudinally and transversally criss-crossed (Fig. 8(b)-(d)).

To quantitatively illustrate strain relaxation process and behavior of dislocation in Ge donor wafer, a kinetic calculation model is constructed based on theory of Dodson [33], Houghton [41], and Alexander [42]. Different from previous studies, the excess stress is correlated with the thermal strain instead of the lattice misfit. Moreover, strain relaxation process in Ge will be resolved in this our model where nucleation, glide, multiplication, and interaction of dislocations in bonded pairs are incorporated.

In strained diamond-phase structures, especially Ge with moderate critical resolved shear stress (CRSS), plastic deformation [43] will occur as a response to high excess stress τ_{ex} which can be given by

$$\tau_{\mathrm{ex}} = \tau_{\mathrm{r}} - \tau_{\mathrm{l}} - \tau_{interal} \tag{3}$$

where τ_r is the resolved shear stress, τ_l is line tension of extending dislocations, and $\tau_{interal}$ is internal stress of dislocation network. τ_r and τ_l are derived from Matthews and Blakeslee's model and can be given by [29]

$$\tau_{\mathrm{r}} = 2Gcos\phi cos\lambda\frac{(1+\nu)}{(1-\nu)}\varepsilon \tag{4}$$

$$\tau_{\mathrm{l}} = \frac{Gbcos\phi}{4H\pi(1-\nu)}\left(1-\nu cos^2\theta\right)ln\frac{\beta H}{b} \tag{5}$$

where G is the shear modulus of Ge, b is amplitude of burgers vector, ϕ is the angle between glide plane and bonded interface normal, λ is the angle between b and direction in the interface which is normal to dislocation line, ν is the Poisson ratio, θ is the angle between burgers vector and dislocation line, β is the factor describing energy of a dislocation core, ε is in-plane strain, and H is the thickness of Ge. $\tau_{interal}$ can be derived by the Taylor relation [42,44] :

$$\tau_{interal} = \frac{Gb}{2\pi(1-\nu)}\sqrt{N} \tag{6}$$

The strain rate can be given by

$$\frac{d\varepsilon}{dt} = VNbcos\lambda + (\alpha_{\mathrm{Si}} - \alpha_{\mathrm{Ge}})\dot{T} \tag{7}$$

The first term represents the strain relaxation caused by dislocation motion where V denotes the dislocation propagation velocity [45]. The second term denotes the thermal strain rate where α_{Si} and α_{Ge} denote the CTE of Si and Ge respectively, and $\dot{T}$ denotes the temperature rate. Relationship between the dislocation velocity V and τ_{ex} can be given by an Arrhenius model:

$$V = V_0 \tau_{ex}^m exp\left(\frac{-Q_v}{kT}\right) \tag{8}$$

where V_0 and m are material constants related to Ge, and Q_v is activation energy for dislocation glide [46,47]. Dislocation nucleation rate is given by

$$\frac{dN}{dt} = BN_0 (\frac{\tau_{ex}}{G})^n exp(\frac{-Q_{nu}}{kT}) + NV\delta \tag{9}$$

where N_0 is the density of "initial nucleation sites", $Q_{nu}$is the activation energy, and B is a material constant. The first term in Eq. (9) represents the nucleation rate, and the second term denotes the multiplication rate [42]. It has to be stressed that specific notion of "initial nucleation sites" density N_0 still remains unclear in previous literatures. Impurity atoms, surface imperfections, and oxide are all conjectured to have an influence on N_0. It is introduced here to act as a parameter that characterizes the integrated influence of surface fluctuations and pretreatment on initial nucleation of dislocation. The multiplication coefficient δ can be given by [42,48,50]

$$\delta = \frac{8\pi(1-\upsilon)}{L} (\frac{\tau_{ex}}{G})^p \tag{10}$$

where L is length of an active Frank-Read multiplication source that can be obtained by solving the equation:

$$b\tau_{ex} = \frac{Gb^2}{4\pi r(1-\nu)} \left\{ \left[1 - \frac{\nu}{2}(3 - 4cos^2\theta)\right] ln\frac{L}{\rho} - 1 + \frac{\nu}{2} \right\} \tag{11}$$

under the equilibrium condition [36,49]

$$r = \frac{L}{2} \tag{12}$$

In Eqs. (11) and (12), r is radius of curvature of a bowing-out loop in Frank-Read multiplication process. Note that, strain relaxation and dislocation nucleation process can be clarified by solving Eqs. (3)-(12) using a time-domain differential method. Key parameters used during the calculation process are tabulated in Table 2.

During the calculation process, the heating and cooling rate are fixed to 0.5 °C min^{-1} which is in accordance with our experiment. As shown in Fig. 9(a), DD in Ge wafer of Ge/Si bonded pair is plotted as a function of annealing temperature. The calculated DD fits the experimental data well when N_0 equals 1×10^5 cm^{-2}. One can see that DD depends strongly on N_0 at low temperature range. This can be attributed to the sluggish motion of dislocations and inhibited interaction among them at low temperature. However, at elevated temperatures, DD overlaps at 1×10^7 cm^{-2} irrespective of N_0 because multiplication process triggered by Frank-Read sources is dominant for dislocation nucleation process. That is consistent with the conclusion reached by Alexander [42] and D. Dew.Huges [50]. The DD predicted by energy equilibrium theory is also plotted in Fig. 9(a) for comparison. The results diverge from the experimental data in the whole temperature range.

Evolution with time of DD at different annealing temperature is plotted in Fig. 9(b). It can be observed that in the whole annealing temperature regime, DD increases rapidly at first and then saturates with reduced nucleation rate. Majority dislocations are nucleated during the constant temperature period of annealing. Nucleation rate increases as temperature goes up, and a rapid growth of DD can be observed at annealing temperatures of 375 °C and 400 °C. Fig. 9(c) shows the evolution with time of strain. Significant acceleration of strain relaxation can be seen in bonded pairs annealed at 375 °C and 400 °C. This is due to the simultaneous booming of dislocation which will notably relieve the thermal strain in Ge. Solid lines in Fig. 9(d) show DD in Ge as a function of prolonged annealing duration at 300 °C and 400 °C . It can be observed that as annealing duration increases, DD saturates rapidly at 400 °C, while increasing moderately at 300 °C. Satisfactory agreement is obtained between the theoretical predictions and experimental data, verifying the accuracy of our model.

It is evident that lowering the annealing temperature is an efficient way to suppress the dislocation nucleation in Ge/Si bonded pairs, and an optimized surface pretreatment is expected to further reduce the nucleation sites at bonded interface. However, low temperature annealing will result in a weakened bonding strength and degraded thermal stability of the bonded pairs. That will readily cause the exfoliation of Ge in subsequent device fabrication process such as the dopant activation, ultrasonic cleaning and the plasma-enhanced chemical vapour deposition (PECVD). Hence, it is suggested that mediating the thermal stress at the Ge/Si bonded interface may offer more efficient solutions, such as patterned interface (usually with high height/width ratio), to lower the DD in Ge [18]. By this way the thermal stress in Ge film may be locally lowered through strain compensation induced by the microstructures at bonded interface. Moreover, according to Eqs. (3)-(5), it is deduced that the excess stress can be reduced by thinning the Ge film thickness at a given strain amplitude. The areal strain density can be lowered simultaneously in thinned Ge film [31]. To transfer ultra-thin Ge film onto Si substrate may serve as another approach to lower the nucleation probability and propagation velocity of dislocation in Ge during the bonding process.

Table 2
Key parameters used in kinetic strain relaxation model in this work.

	Value	Reference
θ(°)	60	60° 1/2 ⟨1 1 0⟩ mixed type
ϕ(°)	35.2	{1 1 1} planes as slip plane of dislocation.
λ(°)	60	
β	4	[31]
V_0($m^2N^{-1}s$)	3×10^{-4}	[47,24]
m	1	[51]
Q_v(eV)	1.6	[43,47,52]
Q_{nu}(eV)	2	[53]
n	2.5	[41,54]
B(s^{-1})	10^{18}	

4. Conclusions

Strain relaxation and behavior of dislocation in Ge/Si bonded pair is investigated. Two types of dislocation network are revealed in Ge donor wafer at different annealing temperature regimes. A thin a-Si intermediate layer is introduced to eradicate the influence of misfit in lattice. The thermal stress is proved to be the driving force for dislocation nucleation. A kinetic model clarifying strain relaxation and dislocation nucleation process in Ge/Si bonded pairs is constructed. By fitting the experimental data, it is proposed that heterogeneous nucleation triggered by unevenly distributed thermal stress is dominant for the dislocation nucleation process at low annealing temperature range, and the DD primarily multiplied through Frank-Read sources at elevated annealing temperatures.

CRediT authorship contribution statement

Donglin Huang: Conceptualization, Methodology, Data curation, Validation, Investigation, Software, Writing – original draft, Writing – review & editing. **Ruoyun Ji:** Validation, Investigation, Formal analysis. **Liqiang Yao:** Investigation, Formal analysis. **Jinlong Jiao:** Formal analysis. **Xiaoqiang Chen:** Formal analysis. **Cheng Li:** Resources, Formal analysis. **Wei Huang:** Resources, Formal analysis. **Songyan Chen:** Supervision, Conceptualization, Writing – review & editing, Funding acquisition. **Shaoying Ke:** Formal analysis, Writing – review & editing, Funding acquisition.

Declaration of Competing Interest

The authors declare that they have no known competing financial

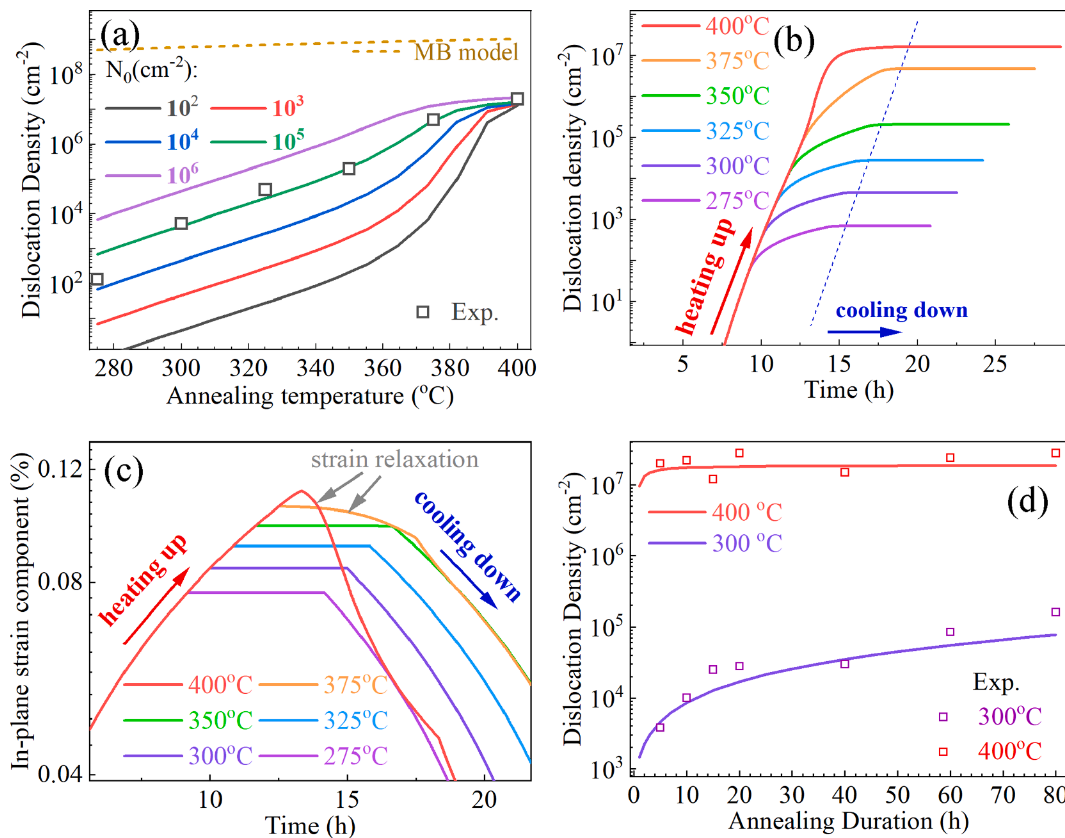

Fig. 9. (a) For different value of N_0, DD in Ge predicted by our model (solid lines) and that obtained in experiments (open squares) versus annealing temperature. DD predicted by energy equilibrium theory is plotted by dashed line. Evolution with time of (b) DD and (c) in-plane strain in Ge during annealing process. (d) DD predicted by our model (solid lines) and obtained in experiments (open squares) versus prolonged annealing duration at 300 °C, and 400 °C.

interests or personal relationships that could have appeared to influence the work reported in this paper.

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